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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/166,496	10/05/1998	HOLGER BELLMANN	10191/821	9214

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EXAMINER	
BROADHEAD, BRIAN J	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/166,496
Filing Date: October 05, 1998
Appellant(s): BELLMANN ET AL.

Gerard A. Messina
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 3, 2007 appealing from the Office action mailed March 1, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,642,756	Sherrod	2-1987

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 12, and 14, are rejected under 35 U.S.C. 102(b) as being anticipated by Sherrod, 4642756.

As per claim 1 and 12, Sherrod discloses a plurality of activatable modules with corresponding priority values on lines 36-47, on column 1, on lines 7-26, on column 2, and on lines 14-16 and 35-36, on column 3; a scheduler activating the modules as a function of the corresponding priority values on lines 7-22, on column 3, on lines 11-16, on column 4, and on lines 24-25, on column 4; the activatable modules generating data by analyzing the states of the system on lines 1-8 and 38, on column 4 (I/O operations on a computer are tasks that generate an outputs based on inputs); and a priority manager modifying the corresponding priority value of at least one of the modules to one of increase and decrease the respective corresponding priority value relative to the priority value of another of the activatable modules on lines 11-16, 24-25, 35-42, on column 4, and lines 45-48, on column 5.

As per claim 3 and 14, Sherrod discloses the priority manager modifies the corresponding priority of the module as a function of the states of the system on lines 35-37, on column 4.

(10) Response to Argument

Appellant's argues that Sherrod fails to identically disclose every limitation recited in the claims. The first limitation that Appellant addresses is that of "a plurality of activatable modules with corresponding priority values." As disclosed in previous responses to this argument throughout prosecution it has been pointed out that the tasks disclosed in Sherrod are equivalent to the activatable modules. Sherrod discloses these tasks on lines 14-18 and lines 35-37, on column 3, on lines 35-40, on column 4, and many other locations throughout the specification. In Appellant's own specification these "modules" are discloses as being program modules on lines 12-13, on column 3. It is important to note in this section of the specification that the "scheduler" and "priority manager" are also disclosed as being programs (software). These programs that are the activatable modules clear are anticipated by the tasks discloses by Sherrod. The claims also require that the activatable modules generate data by analyzing the states of the system. This limitation has been given a very broad interpretation. Since the tasks discloses in Sherrod are performing I/O operations (line 37, col. 4), and all the other function associated with a computer system with the hardware disclosed on lines 1-8, on column 4, it is very clear that the modules are generating data by analyzing the states of the system. In a simple example for any I/O operation, inputs are the states of the system and the outputs are the generated data.

The second limitation that Appellant argues Sherrod fails to disclose is that of "a scheduler activating the activatable modules as a function of the respective corresponding

priority value of each of the activatable modules to provide activated modules." Sherrod discloses an equivalent structure on lines 7-22, on column 3, on lines 11-16 and 24-25, on column 4. This scheduler is disclosed as being part of the logic circuit 7' in Sherrod. This logic circuit is disclosed as containing the instructions and data required to carry out its functions (lines 24-25, col. 4). The functions carried out are further disclosed as the method described on lines 54-58, on column 5. There are two distinct functions disclosed as being part of the method. This would correspond to two distinct set of instructions contained on program logic 7'. This also relates to the next limitations that Appellant argues.

Appellant next argues that Sherrod fails to disclose "a priority manager continuously modifying the respective priority of each of at least one of the activatable modules individually to one of increase and decrease the respective priority value relative to the priority value of another of the activatable modules." The argument made is that the priority manager of Sherrod discloses that the priority manager is contained in the same logic as the task scheduler and they aren't separate elements. It is true that Sherrod does have the task scheduling and priority management as residing in the same logic element, or memory but this does not mean they are the same element. Remember, Appellant discloses the scheduler and priority manager as being "program modules" (lines 12-13, on column 3). Sherrod discloses his logic element 7' as containing the instructions necessary to carry out its functions (lines 24-25, col. 4). The functions are discloses as containing two parts (lines 54-58, col. 5). These two parts are going to have their own sets of instructions that correspond to Appellant's scheduler and priority manager. One way to look at this simply would be to examine an everyday PC. Most PCs have multiple programs on their hard drive such as windows XP, Adobe Acrobat, MS office, etc. Since they are all on the same hard drive would it be proper to call them all one program? Another problem with Appellant's arguments is that the term "program module" is never clearly

defined. Taking the broadest reasonable interpretation one has to conclude that Sherrod's invention reads on the claims as currently written.

Finally, Appellant argues, "the Sherrod reference only states that the internal or external priority changes depending on the computer operator or depending on other events, but not depending on another task and not relative to a priority value of another task." It is important to note that the claims to not recite the underline portion above and that may be where the problem lies. The claims simple claim that when a priority of one task is changed it is relative to another task. This is must happen whenever a task priority is changed in Sherrod. For example, if you have three tasks A, B, and C and they all have priority values A=1, B=2, and C=3. If you increase any priority value it changes the priority relative to all the other tasks. If C=1, then C is now higher in priority than B and has moved relative to A. But even if this is not the case, Sherrod provides a specific example on lines 45-47, on column 5. This example provides for relative priority changes between two tasks and depending on the state of the system

The method claim is not argued separately and it is important to note that not all of the arguments presented by Appellant are applicable to the method claims. For example, there is not a scheduler or priority manager claimed separately for performing the steps of the method.

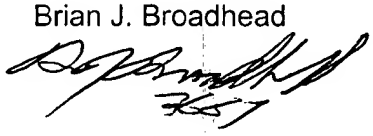
(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Brian J. Broadhead



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EXAMINER	
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Commissioner for Patents

Attached is a corrected Examiner's Answer to the appeal brief filed 1-3-07. The only change is the inclusion of the relaed proceedings appendix. The rejection, arguments and substance of the answer remains the same.

Brian J. Broadhead
Examiner
Art Unit: 3661